1. (Once Amended) A polishing head in an apparatus for chemically-mechanically polishing semiconductor wafers, the polishing head comprising:

(a) a first side having at least a portion thereof operably connectable with a spindle on the apparatus; and

B1 (b) a second side opposite the first side, the second side having a substantially spherical cap shape comprising an outer region adapted to apply a first force onto a semiconductor wafer against a polishing pad, and an inner region adapted to apply a second force onto the semiconductor wafer against the polishing pad, the first force being greater than the second force, and wherein the first force and the second force cause the polishing pad to planarize the semiconductor wafer substantially uniformly.

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9. (Once Amended) A method of polishing a semiconductor wafer in a chemical mechanical polishing apparatus, the method comprising:

(a) providing a chemical mechanical polishing apparatus having a polishing head comprising a first side having at least a portion thereof in contact with a spindle on the apparatus, and a second side opposite the first side, the second side having a substantially spherical cap shape comprising an outer region and an inner region;

B2 (b) securing the semiconductor wafer in the polishing head, the semiconductor wafer having a center region and a perimeter region;

(c) inserting a polishing pad in the apparatus;

(d) applying a first force using the outer region of the spherical cap shape, the first force tending to press a perimeter region of the semiconductor wafer against a polishing pad;

(e) applying a second force using the inner region of the spherical cap shape, the second force tending to press a center region of the semiconductor wafer against the polishing pad, the first force being greater than the second force; and

(f) polishing the semiconductor wafer such that the first force and the second force cause the polishing pad to remove semiconductor surface at substantially the same rate in the center region and in the perimeter region of the semiconductor wafer.
